AMENDMENTS TO THE SPECIFICATION

All amendments are made with reference to the present application as originally filed.

1) Please amend the paragraph beginning on page 8, line 27 of the specification as follows:

The discussion so far has also been primarily in terms of a circuit or gate 10 having one desirable function f and either one or two voltage range(s) for the analog control or configuration voltage A for which the function is undesirable or indeterminate. However, as is disclosed in the aforementioned copending application number 10/526,613 ~~_____~~, useful polymorphic gates can be made using evolutionary algorithms (EA) that are used to create embodiments of electronic circuits using varying topologies of transistors, various transistor lengths and widths. Each such embodiment of a polymorphic gate is defined as a netlist which describes the network of connections between transistors in a simple form. An embodiment created by the EA has a feature that when fabricated yields perhaps only one particular digital function f, but more preferably a range functions f_0, f_1,... f_n each separated by regions of indeterminate operation x as function of the magnitude of the analog control or configuration voltage A.

2) On page 5 of the specification, after line 8 but before the wording "Detailed Description of the Invention", please add the following paragraphs:

Figure 15 is a depiction of two gates each having a single function f having an associated configured range (Ac_{min} to Ac_{max}).

Figure 16 shows a plot of the likelihood of a distribution with the same sigma as the distribution shown in Figure 11, producing two identical finger prints and plotted as a function of the number of boundaries in the system.